Comparative Study of FinFETs versus 22nm Bulk CMOS technologies: SRAM Design Perspective

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***Abstract*—In this paper, FinFET devices are compared to bulk CMOS technology by looking at the characteristics of both devices and their challenges in nano-scale regimes. The effects of process variations on these devices along with the effect of device parameters on their characteristics are explored. Both FinFET and CMOS devices are used in 6T and 8T-SRAM cells. Simulation results show significant improvements for FinFET-based SRAMs compared to bulk CMOS-based SRAM cells. FinFET based 6T-SRAM cell shows 39% improvement in read static noise margin, 54% higher write margin, 54% smaller minimum supply voltage applicable, and 7.3X less leakage power compared to its CMOS counterpart. 8T-SRAM using FinFET improved read static noise margin, write margin, minimum supply voltage and leakage power consumption by 7%, 64%, 50%, and 3.1X compared to bulk-CMOS 8T-SRAM, respectively.**

Keywords—FinFET; SRAM; CMOS;

I. INTRODUCTION

Bulk CMOS technologies have been the cornerstone of semiconductor devices for years. Moore's law motivates the technology scaling in order to improve the performance features such as speed, power consumption and area. While circuit and systems take the advantages of inevitable scaling down the technology, the effect of undesired features such as short channel effects (SCEs) and sensitivity to process variations has been increased [1]-[3]. The short channel effects include the limitation imposed on electron drift characteristics in the channel and the threshold voltage variation along with I_{ON}/I_{OFF} reduction and leakage current increase have been caused the use of bulk CMOS transistors in sub 22nm technologies impossible. It is due to the fact that I_{ON}/I_{OFF} reduction causes instability and limits subthreshold circuit design. On the other hand, leakage current increment increases static power consumption.

SCEs can be reduced by using thinner gate oxide, while it will lead to a higher gate leakage current exponentially due to tunneling. It increases total power consumption and reduces device reliability. Thus, new transistor structures have been proposed in order to overcome the SCEs [4]-[8]. Among different proposed devices, FinFET is one of the best candidates in order to overwhelm the restrictions of bulk CMOS technologies toward deep nano-scale technologies. What makes FinFET different from bulk CMOS transistor is the thin silicon fin that plays the role of channel and conducts the electron carriers between source and drain. Fig. 1 shows the different structures of FinFET. As shown, the channel is surrounded from three dimensions by gate results in a superior

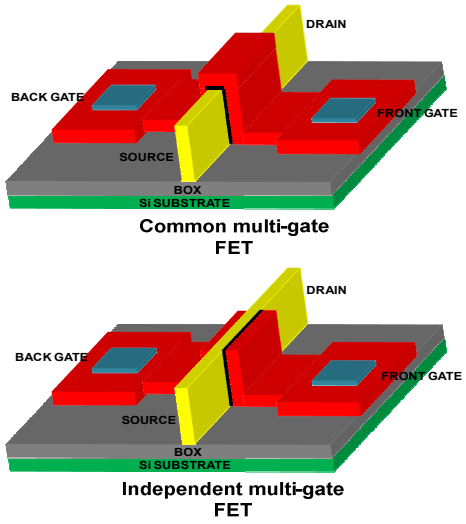

Fig. 1. Different structures of FinFET [8]

control of the channel. Furthermore, it decreases the SCEs and eliminates random dopant fluctuation (RDF) effect due to fully depleted channel that causes less sensitivity to process variations [9].

One class of circuits affected critically by the scaling issues is the static random access memory (SRAM) [10]. It is due to using minimum size transistors in SRAM structures in order to minimize the area overhead that increases the sensitivity to process variations. Besides, considering the fact that most of cells in SRAM array are inactive, leakage currents contribute to a large part of total power consumption.

In this paper, we compare different features of bulk CMOS transistors with FinFET and the effect of utilizing these two types of transistors on reliability and power consumption of SRAM structure will be explored. The rest of this article is arranged as following: in section II, the features of bulk CMOS transistor are compared with FinFET. In section III, reliability and power consumption of 6T and 8T SRAM cell while using FinFET and bulk CMOS technology in 22nm technology are explored. Finally, the results are included in section IV.

II. BULK CMOS VERSUS FINFET

In this section, different features of a bulk CMOS transistor in 22nm technology are compared with a FinFET transistor in 20nm technology. 24nm channel length for both transistors is

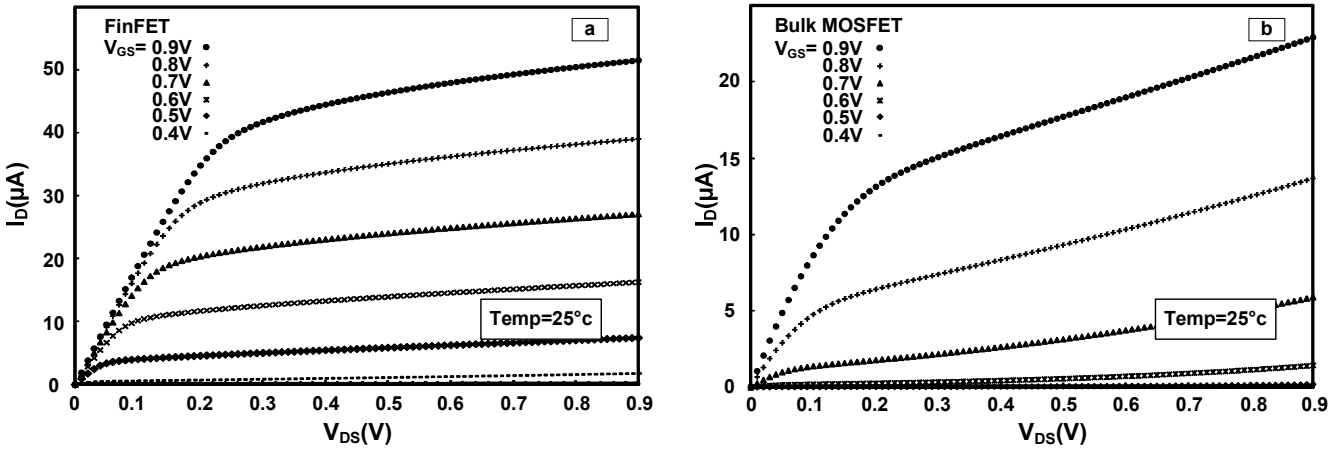

Fig. 2. The I-V characteristic of (a) FinFET (b) bulk CMOS transistors

used. The width of bulk CMOS transistor is 71nm while the fin height and fin thickness of FinFET transistor are 28nm and 15nm, respectively, that makes its width equal with bulk CMOS transistor. Table I shows the characteristics of FinFET transistor that is used. All simulations have been performed in HSPICE using Predictive technology models (PTMs) [11].

A. I-V characteristic

Fig. 2 shows I_D versus V_{DS} for bulk CMOS and FinFET transistors when V_{GS} changes from 0V to 0.9V. Two features can be derived from strong inversion region including the level of ON current and output resistance. The level of ON current in FinFET is higher. Besides, it has higher output resistance (less channel length modulation). It is due to the fact that the channel is surrounded in three dimensions in FinFET. It causes better gate control in this type of transistor.

Fig. 3 shows I_{ON}/I_{OFF} ratio versus supply voltage for both devices. As illustrated, in low supply voltages the I_{ON}/I_{OFF} ratio is higher for FinFET while in high supply voltages (higher than 0.72V) it is higher for bulk CMOS. It is due to the fact that bulk CMOS has a lower I_{OFF} compared with FinFET while FinFET has a higher I_{ON}. In low supply voltages the OFF current of bulk CMOS is lower but it is closed to FinFET while the ON current of FinFET is much higher than bulk CMOS. As a result, the I_{ON}/I_{OFF} ratio is higher for FinFET. However, in high supply voltages (higher than 0.72V) the ON current of bulk CMOS is getting close to the ON current of FinFET and the I_{ON}/I_{OFF} ratio of devices are closed to each other.

B. Drain Induced Barrier Lowering

Fig. 4 shows how the drain current of bulk CMOS and FinFET transistors change versus gate source voltage at V_{DS}=0.1V and V_{DS}=1.1V. Drain induced barrier lowering (DIBL) for bulk CMOS transistor is 124mV/V that is much higher than FinFET (58mV/V). It shows lower threshold voltage variation due to short channel effects for FinFET. Another point derived from the figure is the lower threshold voltage of FinFET (0.36V) than bulk CMOS (0.55V) that is one of the reasons behind the higher level of I_{ON}/I_{OFF} ratio.

TABLE I. FINFET PARAMETERS [11]

Technology(nm)	20
Lg(nm)	24
EOT(nm)	1.1
Tfin(nm)	15
Hfin(nm)	28
NSD(cm-3)	3e26
VDD(V)	0.9
SS(mV/decade)	71
DIBL(mV/V)	58

C. Subthreshold Swing

Fig. 4 also shows that the subthreshold swing (SS) of the FinFET is 21% lower than bulk CMOS transistor at room temperature. It shows more dependency of the drain current to V_{GS} in FinFET transistor. Considering the subthreshold I-V relation where drain current changes exponentially with V_{GS} [12], it shows that the dependency of drain current with V_{GS} in FinFET increases in a faster pace than bulk CMOS.

Fig. 5 shows the effect of temperature on SS. Temperature is changed from -40°c to 125°c and SS is calculated for both

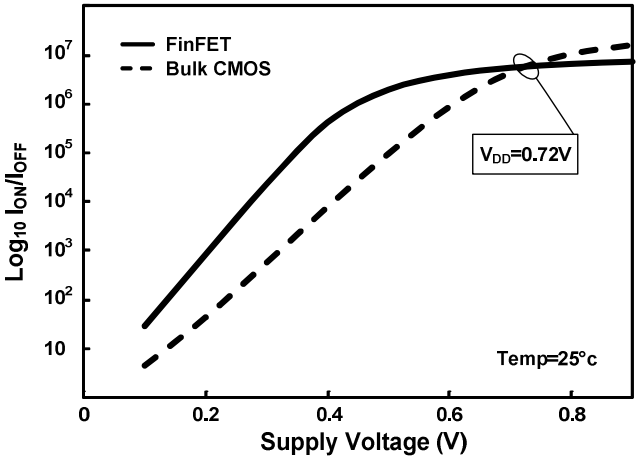

Fig. 3. I_{ON}/I_{OFF} ratio versus supply voltage for FinFET and bulk CMOS transistors

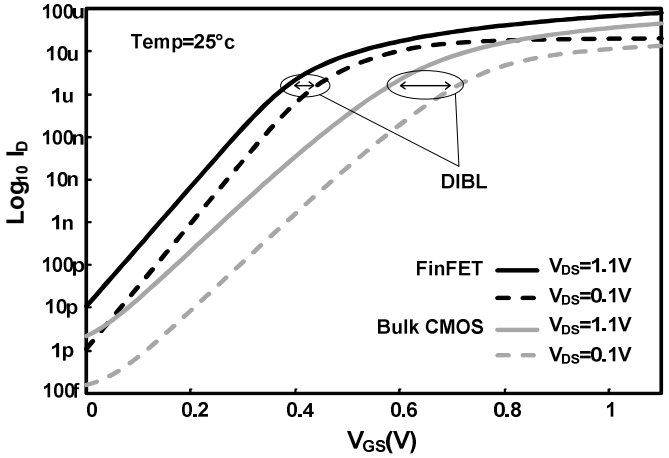

Fig. 4. Drain current versus Gate Source voltage for FinFET and bulk CMOS while V_{DS} is 0.1V and 1.1V

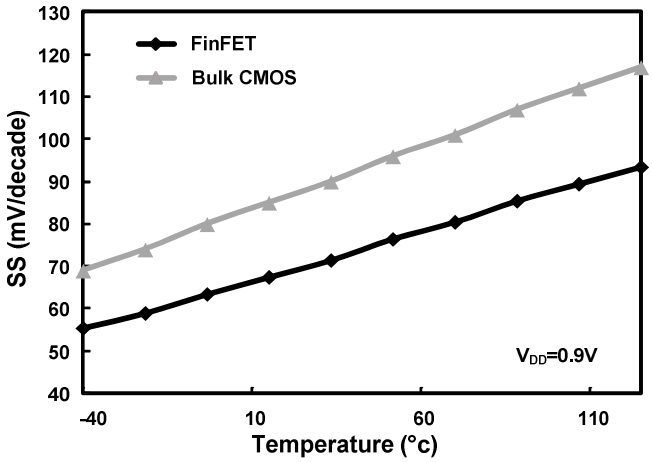

Fig. 5. Subthreshold swing versus temperature for FinFET and bulk CMOS

devices. As illustrated, SS is increased as temperature is raised linearly for both devices. However, the rising rate of SS for bulk CMOS is higher than FinFET. It shows more sensitivity of SS to temperature in bulk CMOS.

D. Gate Induced Drain Leakage

Gate leakage in nano-scale bulk CMOS transistor is one of the most important concerns. In order to calculate the gate induced drain leakage (GIDL), V_{GS} has to sweep from negative voltages to positive voltages as shown in Fig. 6. As it is clear from this figure, the behavior of FinFET is different from bulk CMOS for negative V_{GS} and it shows a better GIDL. Using negative V_{GS} decreases subthreshold current in both devices. However in bulk CMOS, it is constant at $V_{GS} < -0.1V$ and starts to increase rapidly at $V_{GS} < -0.3V$ that is attributed to increased gate leakage.

E. Channel Length Effect

Fig. 7 shows drain current versus V_{GS} for different channel lengths (L_{CH}) from 24nm to 54nm. It shows faster decrease in I_{OFF} for FinFET compared with bulk CMOS by increasing L_{CH} while I_{ON} is sort of constant for FinFET but it decreases for Bulk CMOS. It can be used in order to reduce leakage power consumption at cost of increasing the area and lower I_{ON}.

Another point derived from Fig. 7 is the less dependency of threshold voltage to L_{CH} variation in FinFET compared to bulk CMOS. It is highlighted in Fig. 8 where the threshold voltage versus L_{CH} variation has been shown for both devices. Increasing in L_{CH} from 24nm to 54nm caused 14% and 7% increase in the threshold voltage for bulk CMOS and FinFET, respectively. It proves less dependency of FinFET

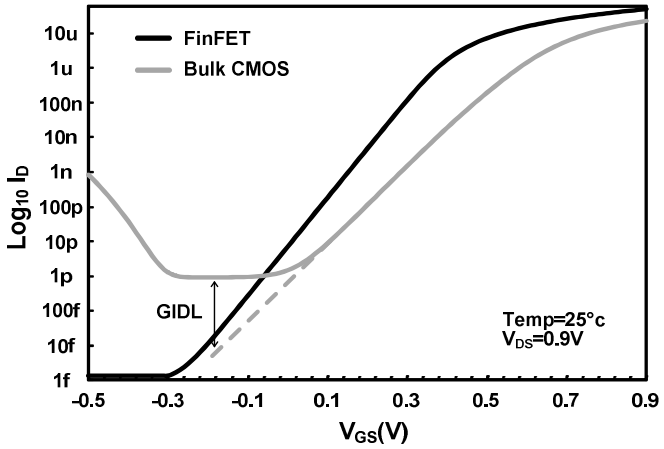

Fig. 6. Drain current versus gate source voltage while drain voltage is V_{DD}

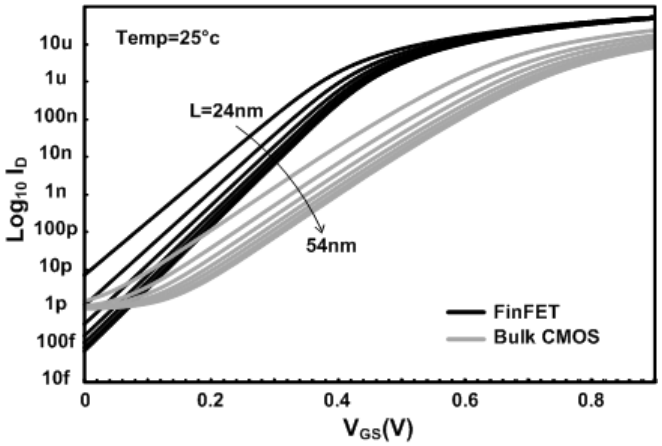

Fig. 7. Drain current versus gate source voltage, while drain voltage is V_{DD} for channel length from 24nm to 54nm

characteristics to process variation.

F. Silicon Thickness Variation

Fig. 9 shows I_{ON}/I_{OFF} ratio variation due to silicon thickness (T_{SI}) variation from 7nm to 15nm. As it is illustrated, the I_{ON}/I_{OFF} ratio increases dramatically by decreasing T_{SI}. I_{OFF} decreases by 50% with 1nm reducing in T_{SI} for FinFET while I_{ON} is degraded by 1.5%. This feature can be used for reducing the leakage current in FinFET. However, it has to be considered that there is a minimum thickness applicable (due to physical stability issues) in each technology.

G. Fin Height Variation

Fig. 10 shows I_{ON} and I_{OFF} versus fin height (H_{FIN}) variation. As it is illustrated, 11% increase in H_{FIN} raises I_{ON}

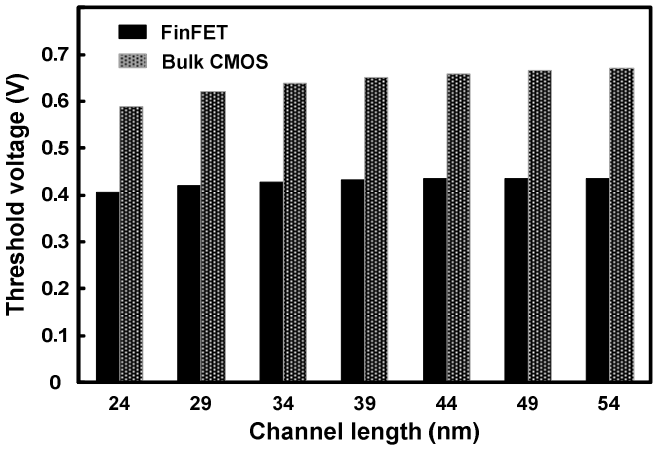

Fig. 8. Threshold voltage versus channel length for bulk CMOS and FinFET

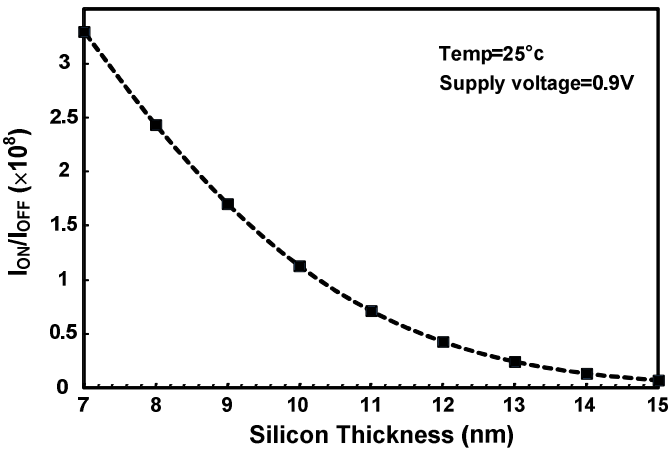

Fig. 9 I_{ON}/I_{OFF} ratio for different silicon thickness

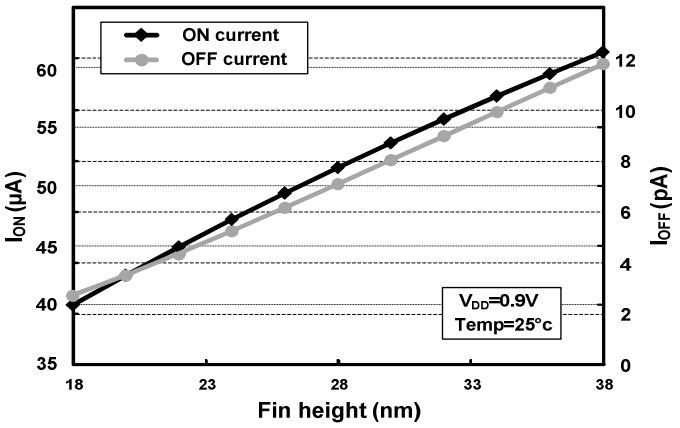

Fig. 10. I_{ON} and I_{OFF} versus fin height

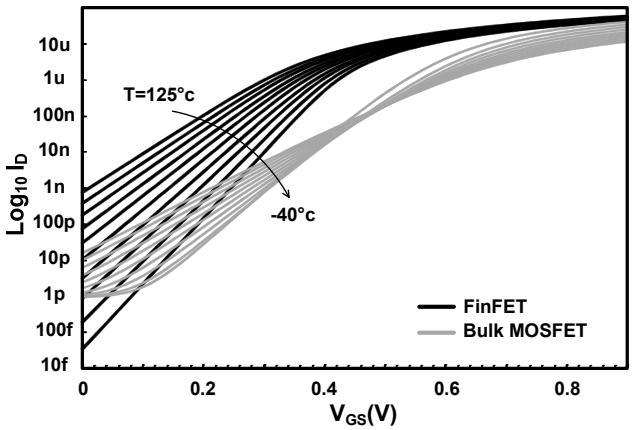

Fig. 11. Drain current versus Gate Source voltage for different temperatures for FinFET and bulk CMOS

and I_{OFF} by 6% and 29%, respectively. Therefore, increasing the fin height is not a good way in order to achieve a higher I_{ON} for low power applications due to the fact that higher fin height increases I_{OFF} more than I_{ON}. However it has to be considered that increasing H_{FIN} in FinFET compared with increasing the width in bulk CMOS occupies very small area. This small area penalty is due to the fact that higher fin needs higher thickness in order to physical stability issues. Therefore, increasing the ON current by increasing the fin height causes a negligible area penalty compared to increasing the width in bulk CMOS. This is a very important feature in applications need high density such as SRAMs. SRAMs use excessive number of bit cells in their structures. Therefore, the area occupied with each bit cell has to be at minimum level in order to achieve high density.

H. Temperature

Fig. 11 shows I_D versus V_{GS} for different temperatures (T) vary from -40°c to 125°c. As shown, T variation in bulk CMOS changes both of the performance (I_{ON}) and the leakage power consumption (I_{OFF}) compared with FinFET that it only changes I_{OFF}. However, OFF current variation in FinFET is more severe. Another feature that is affected by temperature variation is threshold voltage. Increasing the temperature from -40°c to 125°c decreases the threshold voltage by 10% and 16% for bulk CMOS and FinFET respectively. It shows more threshold voltage dependency to the temperature in FinFET.

III. 6T AND 8T SRAM CELL

Several SRAM cells have been proposed in order to reach different design goals such as low power consumption, low density, lower supply voltage, and high reliability [13]-[14]. Among them 6T and 8T SRAM cells are the most commonly used cells. Fig. 12 shows 6T and 8T SRAM cell structures. As shown, 6T SRAM cell (a) consists of two back to back inverters (PU1-PD1 and PU2-PD2) that keep the data and its inverse in nodes Q and QB, respectively. The access transistors (AC1-AC2) are used to perform read and write operations. Due to common path for read and write operations, there are design trade-offs in the strength of transistors in 6T SRAM cell. While reading the cell, pull down transistors (PD1-PD2) stronger than access transistors (AC1-AC2) increase the reliability of the cell. In the other way, when performing the write operation stronger access transistors than pull down and pull up transistors ease the operation. In the hold mode, equal strength for pull up and pull down transistors ensures the most reliability.

Due to a very high process variation and low noise margin of 6T SRAM, 8T-SRAM cell is used with separate lines for read and write [15]-[17]. This obviates the trade-off between read and write cycles. To make it more clear, stronger access transistors are required in order to improve write margin, while for improving read margin weaker access transistors are needed. This means, this issue can be resolved by separating read and write paths. Fig 12-b shows 8T SRAM cell structure. It consists of a 6T SRAM cell together with a read circuit (R1-R2 transistors and RBL line). The write operation is done by BL and BLB lines througth access transistors (AC1-AC2). R1 and R2 transistors are used in order to make the data stored in node Q on RBL line during read operation. This structure obviates the trade-offs between read and write.

Since most of SRAM cells are in standby mode, the leakage current is one of the main concerns for SRAM designs. Besides, in order to reach the maximum density in SRAM memory, minimum width transistors are used. Minimum size transistors along with accurate sizing ratio of transistors requirements make SRAM cell reliability very sensitive to proccess variations. In this section, the effect of using FinFET and bulk CMOS transistors on power consumption and robustness of 6T and 8T SRAM cells are explored. In order to include process variation due to RDF on RSNM, WM, and supply voltage scalability simulations, □(V_{TH}) of 25mV and 28mV for n-channel and p-channel FinFETs and □(V_{TH}) of

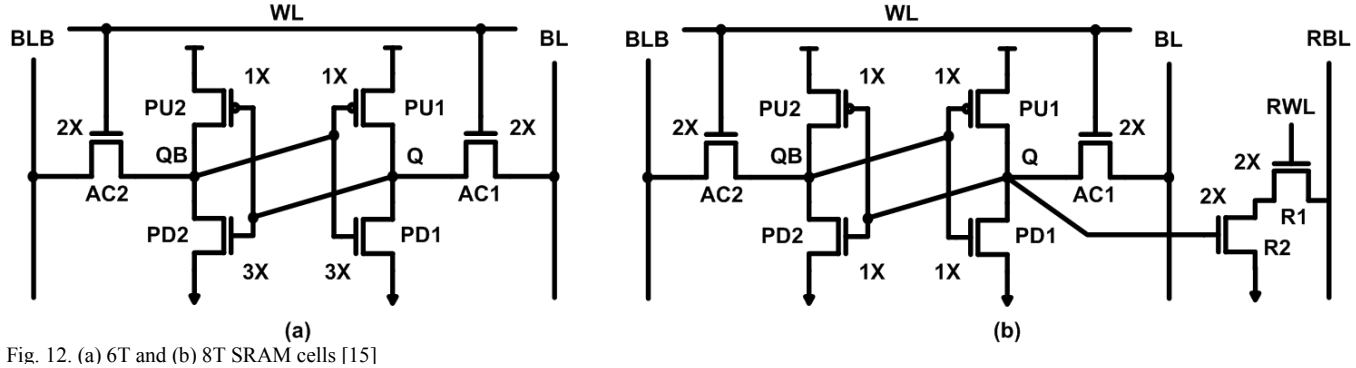

Fig. 12. (a) 6T and (b) 8T SRAM cells [15]

45mV and 49mV for NMOS and PMOS have been considered [18] and a Monte Carlo analysis with 1000 itterations is performed. 25°C and V_{DD}=0.9V conditions have been considered in whole simulations. Simulations are done using HSPICE with PTM models 22nm LP and 20nm LSTP for bulk CMOS and FinFET transistors, respectively.

A. 6T SRAM cell

1) RSNM: Read static noise margin (RSNM) is a metric showing read stability of a SRAM cell. It is defined as the length of the side of the largest square that can fit into the lobes of the butterfly curve. Butterfly curve is obtained by drawing and mirroring the inverter charachteristics while access transistors are ON and bitlines are precharged to V_{DD} [19]. The size of transistors has shown in Fig. 12. The parameter X is W/L ratio for bulk CMOS transistors that is 71nm/24nm (e.g., the size of PD2 in 6T SRAM is 3X or W=213nm/L=24nm). When using FinFET transistors X=1 and the term shows the number of fins (e.g., the number of fins for AC1 is 2).

Fig. 13 shows the RSNM of 6T SRAM cell. As shown, RSNM variation while using FinFET is much lower than bulk CMOS. This is due to less threshold voltage variation in FinFET. The mean value and variance of RSNM are 229mV (173mV) and 2.66×10^{-06} (1.88×10^{-05}) for FinFET (bulk CMOS). The RSNM values are 223mV and 160mV for FinFET and bulk CMOS, respectively. It shows 39% improvement for FinFET 6T-SRAM cell.

2) Write Margin: Write margin (WM) is a measure of writeability of a SRAM cell. There are several methods in order to calculate write margin [20]-[22]. Among them, the method used in [22] is used here that shows the effect of strengthening the access transistors on writeability of the cell more accurately.

Fig 14. shows the results of Monte Carlo analysis for WM. The mean value and variance of WM are 295mV (209mV) and 3.521×10^{-05} (1.11×10^{-04}) for FinFET (bulk CMOS). Write margin is obtained 180mV and 278mV for bulk CMOS and FinFET, respectively. It shows 54% improvement in WM for FinFET structure.

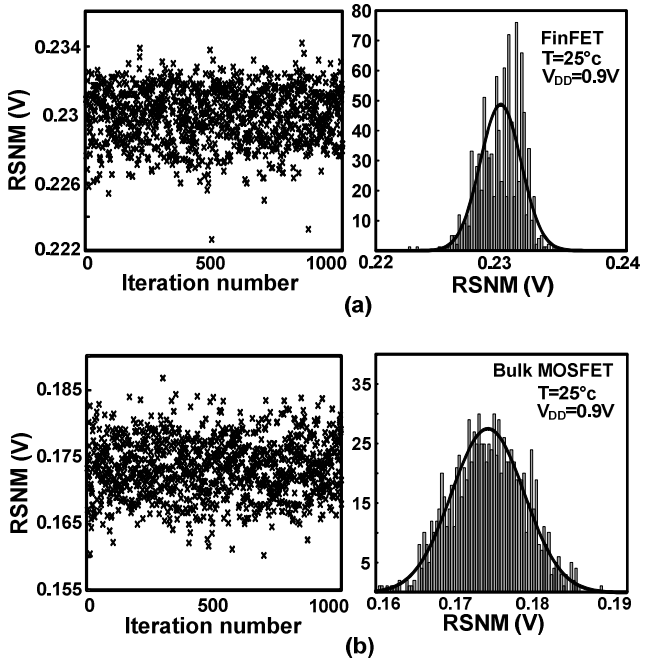

Fig. 13. Monte Carlo analysis of RSNM in 6T SRAM cell for threshold voltage in presence of process variation for (a) FinFET and (b) bulk CMOS

3) Supply Voltage Scalability: In order to evaluate supply voltage scalability for low voltage applications such as biomedical applications, the Monte Carlo analysis while V_{DD} is swept from 0.95V to 0.2V is performed and RSNM is calculated. As expexcted, RSNM decreases with V_{DD} scaling. By supposing the minimum allowable RSNM is 15% of VDD, the minimum operational supply voltage will be 0.3V and 0.65V for FinFET and bulk CMOS, respectively. It shows that FinFET transistor is a better candidate for low voltage applications.

4) Power Consumption: Leakage Power consumption is calculated for a cell in a 6T-SRAM array with 256 cells in a column. Leakage current is calculated in the same RSNM for both devices. The resault shows that the leakage power consumption of a cell in standby mode is 530pW and 72pW for bulk CMOS and FinFET, respectively. It shows 7.3X more leakage power consumption for bulk CMOS than FinFET.

B. 8T SRAM cell

1) RSNM: In order to calculate the RSNM for 8T SRAM cell, butterfly curve is obtained by drawing and mirroring the inverter charachteristics while access transistors are OFF, RBL is precharged to VDD and R1 is ON.

Fig. 16 shows RSNM of 8T SRAM cell in presence of process variation. RSNM is calculated as 375mV and 352mV for FinFET and bulk CMOS, respectively. 8T SRAM cell RSNM improvement is due to separated read and write lines allowing RSNM to improve upto Hold static noise margin (HSNM). The mean value and variance of RSNM are 379mV (358mV) and 1.38×10^{-6} (1.66×10^{-06}) for FinFET (bulk CMOS).

2) Write Margin: The same method used for 6T SRAM writeabillity is performed for 8T SRAM cell. Fig. 17 shows the result of Monte Carlo analysis for write margin. The mean value and variance of WM are 365mV (247mV) and 4.1×10^{-5} (1.28×10^{-4}) for FinFET (bulk CMOS). The write margin is obtained 344mV and 210mV for finFET and bulk CMOS, respectively. It shows improvement in both FinFET and bulk CMOS 8T SRAM cell write abillity. It is due to stronger access transistors than pull down transistors in 8T SRAM cell compared with 6T SRAM cell.

3) Supply Voltage Scalability: The RSNM of 8T SRAM cell while supply voltage is swept from 0.95V to 0.2V for 8T SRAM cell is calculated. As expected the RSNM is decreased by decreasing the supply voltage. Again, if suppose that the minimum allowed RSNM is 15% of VDD, the minimum source voltage is 0.15V and 0.3V for FinFET and bulk CMOS, respectively.

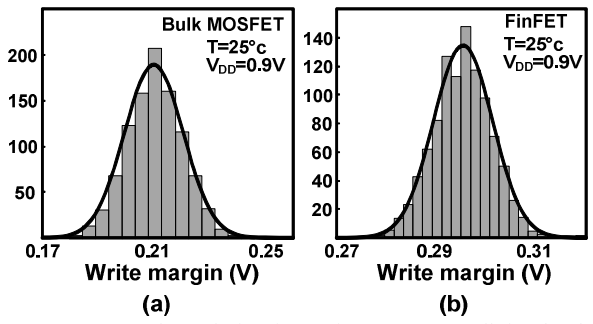

Fig. 14. Monte Carlo analysis of WM in 6T SRAM cell for threshold voltage in presence of process variation for (a) bulk CMOS and (b) FinFET

4) Power consumption: Leakage Power consumption is calculated for a cell in a 8T-SRAM array with 256 cells in a column. The same area is considered for FinFET and bulk CMOS SRAM. The resault shows that the leakage power consumption of a cell in standby mode is 165pW and 53pW for bulk CMOS and FinFET, respectively. It shows 3.1X more leakage power consumption for bulk CMOS than FinFET in the same area. It has to be considered that in this situation the FinFET 8T-SRAM RSNM is 18% higher than the bulk CMOS 8T-SRAM RSNM.

IV. CONCLUSIONS

In this paper, a comprehensive comparison between FinFETs and 22-nm bulk CMOS has been done to observe the challenges and the potentials of using FinFET and traditional bulk CMOS technologies for future electronic devices. Results showed, FinFETs are the promising replica especially for applications for which lowest process variations, lowest leakage power consumption is crucial. Both FinFET and bulk CMOS transistors were used in designing 6T-SRAM and 8T-SRAM to investigate their challenges and potentials for future SRAM architectures. Using FinFET, certainly, outperforms bulk CMOS counterpart for SRAM array design in terms of robustness, power consumption, and reliability.

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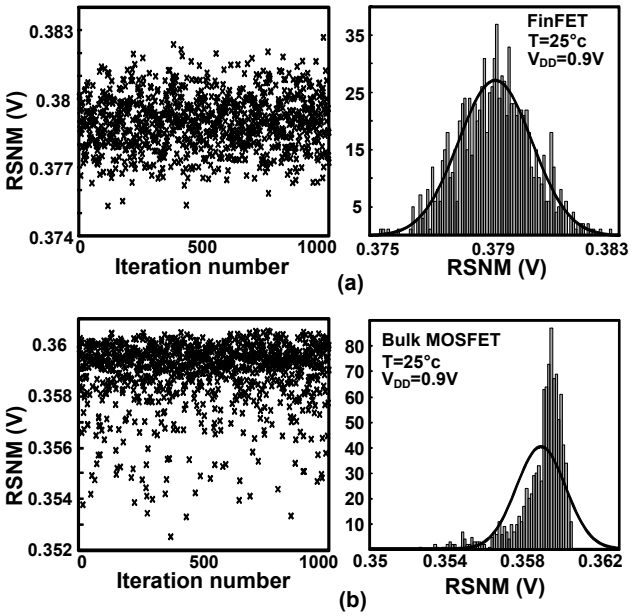

Fig. 16. Monte Carlo analysis of RSNM in 8T SRAM cell for threshold voltage in presence of process variation for (a) FinFET and (b) bulk CMOS

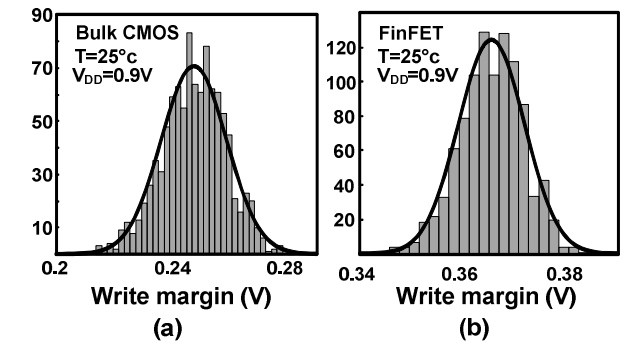

Fig.17. Monte Carlo analysis of WM in 8T SRAM cell for threshold voltage in presence of process variation for (a) bulk CMOS and (b) FinFET